

Final report for proposal:

Towards low-noise microwave amplifiers with outstanding room-temperature noise performance:
development of strained-barrier high electron mobility transistors with improved quantum confinement

Proposal Budget Amount: \$200,000

Period of Performance: March 1, 2023 - February 28, 2025

Related KISS Study Topic Area: The First Billion Years

Name of Campus PI: Austin J. Minnich, Professor of Mechanical Engineering and Applied Physics

Email of campus PI: aminnich@caltech.edu

Telephone of campus PI: 626-395-2142

Division name: Engineering and Applied Science

Co-Investigators:

Kieran Cleary, kcleary@astro.caltech.edu, 626-395-3013

Anthony Readhead, acr@astro.caltech.edu, 626-395-4972

Jacob Kooi, jacob.w.kooi@jpl.nasa.gov, 626-658-1313

Pekka Kangaslahti, pekka.p.kangaslahti@jpl.nasa.gov, 818-393-4492

Overview - The objective of this research is to investigate how high electron mobility transistors (HEMTs) with outstanding microwave noise performance can be achieved by suppressing a noise source, real-space transfer noise, associated with the semiconductor heterojunction. This advance will be achieved by incorporating a strained barrier layer into the epitaxial stack so as to improve the quantum confinement of electrons in the channel.

Summary of achievements – Over the project, we successfully developed a process to fabricate HEMTs at the Kavli Nanoscience Institute using the standard epitaxial film compositions. Further, we obtained strong evidence for the physical origin of the channel noise source as arising from real-space transfer, and that this noise source can be suppressed by increasing the Al composition in the InAlAs barrier. This modification increases the quantum confinement of electrons in the InGaAs channel and thereby inhibits hopping of electrons between the channel and barrier. This work paves the way for continued development of low-noise HEMTs based on strained barriers.

HEMT fabrication process – We developed a fabrication process for HEMTs in the first year and refined it in the second year. It consists of the following steps. First, we write alignment markers and Ohmic contacts using electron beam lithography and electron beam evaporation of a Ti/Pt/Au metal stack. After lifting off, mesas are formed using photolithography and wet etching based on citric acid:H₂O₂ (7:1) for InGaAs, HCl:H₂O (3:2) for InP etch stop, and H₃PO₄:H₂O₂:H₂O (3:1:50) for the InAlAs. After reaching the final etch depth of ~ 30 nm, a highly selective succinic acid:H₂O₂ (9:2) is used, which has a selectivity of $\sim 23:1$ for GaInAs over AlInAs, which laterally undercuts the channel to prevent shorting between the channel and eventual overlay metallization layer.

After this step, the overlay metallization is performed by photolithography and evaporation of Ti/Au to provide metal pads for device probing. At this time, devices can be probed to ensure good Ohmic contacts. Next is the formation and deposition of the gate. The step begins by using electron beam lithography to pattern the T-gate structure in a tri-layer resist consisting of alternating layers of ZEP520A, LOR, and ZEP520A. The T-gate structure enables short gate lengths of ≤ 100 nm for high-frequency performance and large gate-head sizes required to minimize the gate resistance. Subsequently, the cap is etched using a selective citric acid/hydrogen peroxide wet etch and the gate is deposited by sequentially evaporating Pt/Ti/Pt/Au. Finally, liftoff is performed to complete the gate formation. The last steps of the HEMT fab consist of ALD passivation of alumina and gold plating to facilitate electrical probing. Figure 1 shows current-voltage and microwave gain (S_{21}) at room temperature for fabricated devices.

Investigation of real-space transfer noise – In our previous research, we found evidence that real-space

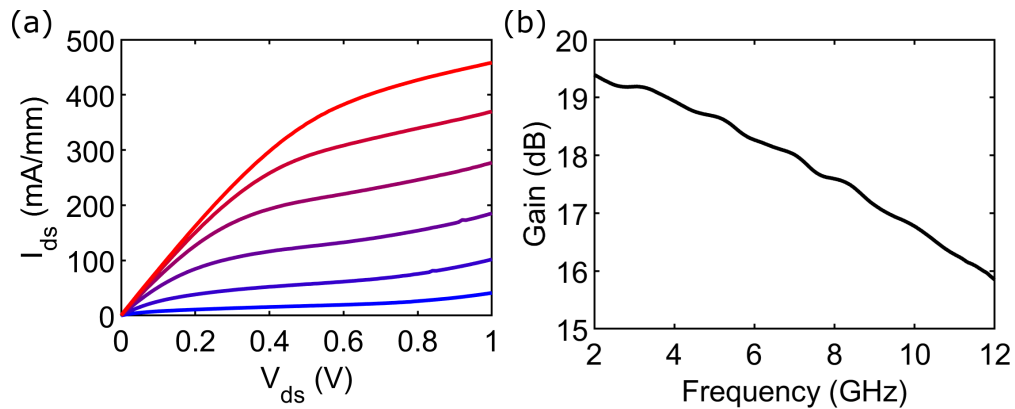


Figure 1: (a) Room temperature I_{DS} - V_{DS} curves of a HEMT fabricated at Caltech. V_{GS} ranges from -0.7 V to -0.2 V. (b) Room temperature S_{21} at optimal bias.

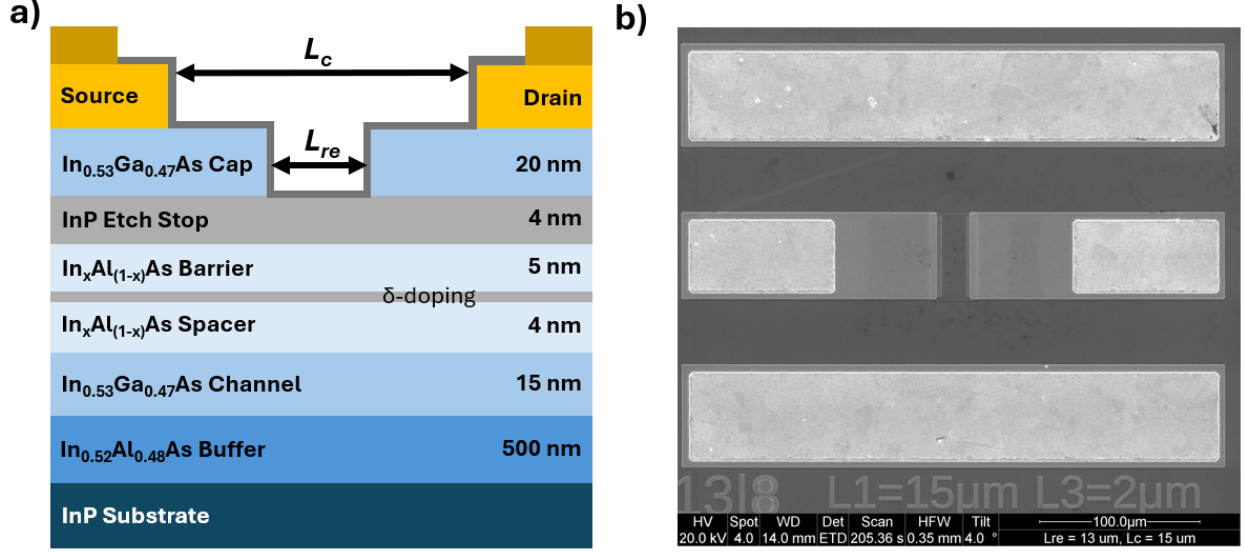


Figure 2: **(a)** Cross section schematic of the ungated HEMT device. The epitaxial layers are grown on an InP substrate. From bottom to top, the epitaxial layers include a 500 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer, a 15 nm $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel, a 9 nm $\text{In}_x\text{Al}_{1-x}\text{As}$ barrier/spacer, a 4 nm InP etch stop, and a 20 nm $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap. The δ doping is located at 4 nm above the channel. A recess with controlled recess length L_{re} is etched on the cap to the etch stop. **(b)** Top view SEM image of the ungated HEMT device. The cross section shown in (a) is located at the center of the device.

transfer noise could be the origin of channel noise detected in HEMTs. The real-space transfer noise mechanism is based on the insight that the electric field can heat high-mobility electrons in the HEMT channel to sufficiently high energy to jump from the channel layer to the lower mobility barrier layer. A key prediction from this theory is that if electrons have higher quantum confinement, they should exhibit less noise compared to electrons in a shallower quantum well. Quantum confinement can be altered (without changing the properties of the channel) by changing the alloy composition of the barrier, $\text{In}_x\text{Al}_{1-x}\text{As}$.

As an intermediate step to realizing HEMTs with improved noise performance, we tested this prediction by characterizing the channel noise of gate-less HEMT structures. In this configuration, we could directly measure channel noise without the complications of additional gate noise. To perform this measurement, we had to make substantial upgrades to our cryogenic probe station to enable noise measurement of lossy devices (rather than HEMTs with gain). These upgrades consisted up modifying the backend which detects the microwave power, introducing pulsed biasing to avoid excessive self-heating, and using cryogenic switches to enable measurement of S-parameters and microwave noise without breaking vacuum.

TLM structures were fabricated on the epitaxial films as shown in Fig. 2a. The wafers were grown by molecular beam epitaxy by IntelliEpi. Two sets of samples were used in which the substrates were identical except for the barrier ($\text{In}_x\text{Al}_{1-x}\text{As}$) Indium composition, x . For the lattice-matched sample (LM), $x = 0.52$, and for the tensile-barrier sample (TB), $x = 0.45$. With these barrier compositions, the conduction band offsets (ΔE_c) of the LM sample and TB samples were calculated as 0.52 eV and 0.66 eV, respectively, using conduction band offsets and bowing parameter values from Vurgaftman et al. As a result, the channel transport properties of each sample are nominally the same, but the electrons have greater quantum confinement in the TB sample.

The substrates were diced into $1 \times 1 \text{ cm}^2$ chips for further processing. Each TLM structure was designed

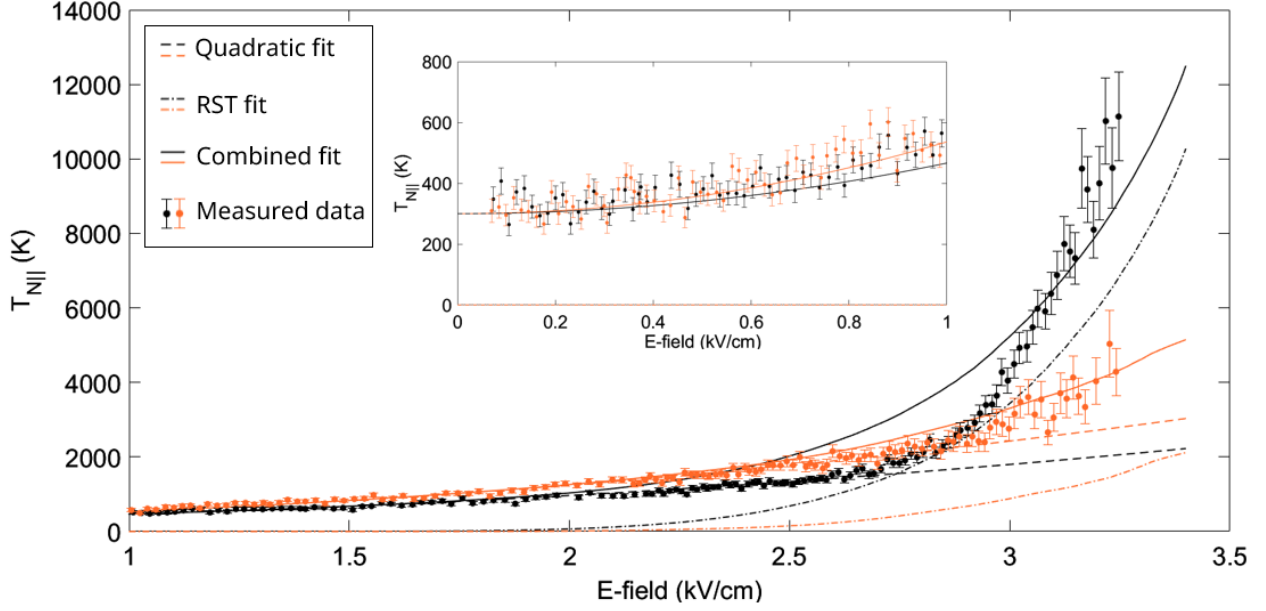


Figure 3: Noise temperature (5 GHz, room temperature) parallel to the channel ($T_{N||}$) of lattice-matched sample (black lines) and strained-barrier (orange lines) versus electric field for a source-drain distance of 13 microns. The dashed lines are the predicted electron temperature considering Joule heating of electrons. The dash-dotted lines are the calculated real-space transfer noise (T_{RST}) from the model proposed by Esho et al. The solid lines are the combined noise temperature predicted both models. The inset shows the low-field region, showing that both fitted model and the measured noise temperature are about 300 K at zero field, as expected.

as a co-planar wave guide (CPW). Figure 2b shows a top view SEM image of the device. The samples were fabricated with various recess lengths (L_{re}) of 1, 3, 8, 13, and 18 μm . The side wall of the recess was fixed to be 1 μm away from the edge of the source and drain metal, such that the distance between the Ohmic contacts (L_c) was 3, 5, 10, 15, and 20 μm , respectively. Two other sets of devices were also fabricated to determine the contact resistance. One set of devices had fixed $L_{re} = 1 \mu\text{m}$ and variable L_c of 3, 5, 10, 15, and 20 μm , while the other set had no recess but the same variation in L_c . The latter set was used to determine the contact resistance and sheet resistivity of the cap layer. With these three sets of devices, contact resistance, and sheet resistances of the cap and channel, as well as the effective channel-barrier resistivity, were determined using the TLM method. These sets of devices were then patterned periodically across the 1x1 cm chip.

Key results from the measurements are shown in Figure 3, which shows the measured noise temperature versus electric field for the two samples. For low enough fields ($\lesssim 2 \text{ kV/cm}$), the noise temperature exhibits a quadratic trend with field, consistent with Joule heating of electrons which is proportional to E^2 . Above around 2.5 kV/cm, a significant increase in noise over this trend is observed for both samples, with the effect especially pronounced for the lattice-matched sample. This observation suggests that electrons in the strained-barrier sample exhibit improved quantum confinement, which inhibits hopping between channel and barrier and hence real-space transfer noise.

These data indicate that there is great potential for improve the noise performance of HEMTs by optimizing the barrier composition to minimize real-space transfer noise while maintaining the high electronic quality of the materials. Research is ongoing in the PI's lab to demonstrate this potential in a HEMT device.